4-Channel, 1kV$_{RMS}$ and 2.75kV$_{RMS}$, Digital Isolators

MAX14930–MAX14932, MAX14130–MAX14131

General Description

The MAX14930–MAX14932 are a family of 4-channel 2.75kV$_{RMS}$ digital isolators utilizing Maxim's proprietary process technology. The MAX14130–MAX14131 are 4-channel 1kV$_{RMS}$ digital isolators in smaller footprint QSOP packages. For applications requiring 5kV$_{RMS}$ of isolation, see the MAX14934–MAX14936. The MAX14930–MAX14932 family transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The MAX14930–MAX14932 family offers all three possible unidirectional channel configurations to accommodate any 4-channel design; including SPI, RS-232, RS-485, and digital I/O applications. For applications requiring bidirectional channels, such as I^{2}C, see the MAX14933.

Devices are available with data rates from DC up to 1Mbps, 25Mbps, or 150Mbps. Each device is also available in either a default high or default low configuration. The default is the state an output goes to when its input is unpowered. See the *Product Selector Guide* and *Ordering Information* for the suffixes associated with each option.

Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX14930–MAX14932 are available in both a 16-pin wide body (10.3mm x 7.5mm) and narrow body (9.9mm x 3.9mm) SOIC package. The MAX14130–MAX14131 are available in a 16-pin (6mm x 5mm) QSOP package. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

***Product Selector Guide* and *Ordering Information* appear at end of data sheet.**

Benefits and Features

- Robust Galvanic Isolation of Digital Signals
  - Withstands up to 2.75kV$_{RMS}$ for 60s (V_{ISO}) (MAX14930–MAX14932)
  - Continuously Withstands 443V$_{RMS}$ (V_{IOWM}) (MAX14930–MAX14932)
  - 630V$_{PK}$ Repetitive Peak Voltage (V_{IORM}) (MAX14930–MAX14932)
  - Withstands ±10kV Surge per IEC 61000-4-5
- Interfaces Directly with Most Micros and FPGAs
  - Accepts 1.71V to 5.5V Supplies
- Many Options Support Broad Applications
  - 3 Data Rates (1Mbps, 25Mbps, 150Mbps)
  - 3 Channel Direction Configuration
  - 2 Output Default States (High or Low)
  - 3 Packages (4mm, 8mm Creepage and Clearance)
- Low Power Consumption at High Data Rates
  At 1.8V:
  - 2.5mA per Channel Typical at 1Mbps
  - 5.25mA per Channel Typical at 100Mbps

  At 3.3V:
  - 2.6mA per Channel Typical at 1Mbps
  - 7.1mA per Channel Typical at 100Mbps

Safety Regulatory Approvals

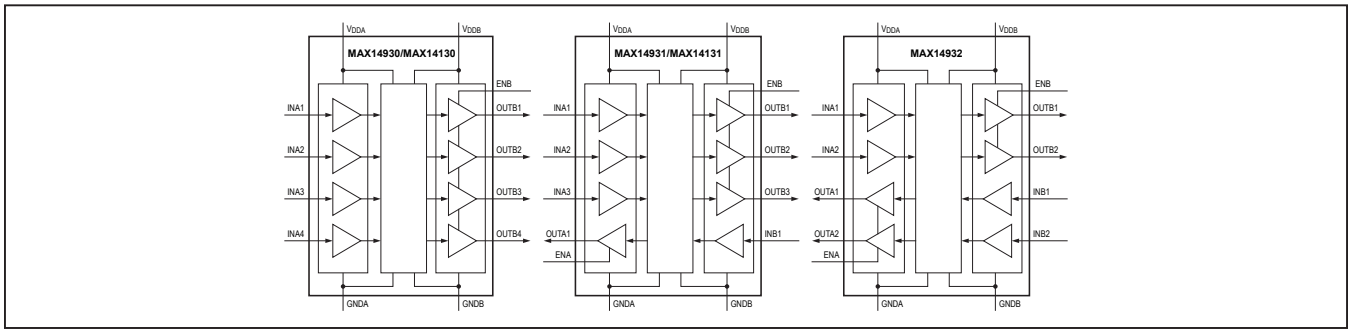
(see Safety Regulatory Approvals)

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-11 Basic Insulation

Applications

- Fieldbus Communications for Industrial Automation
- Isolated SPI, RS-232, RS-485/RS-422
- General Multichannel Isolation Applications
- Battery Management
- Medical Systems

Functional Diagram



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Absolute Maximum Ratings

V_{DDA} to GNDA, V_{DDB} to GNDB .....-0.3V to +6V
INA_, ENA to GNDA.....-0.3V to +6V
INB_, ENB to GNDB .....-0.3V to +6V
OUTA_ to GNDA .....-0.3V to (V_{DDA} + 0.3V)
OUTB_ to GNDB.....-0.3V to (V_{DDB} + 0.3V)
Short-Circuit Duration
(OUTA_ to GNDA, OUTB_ to GNDB) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 14.1mW/°C above +70°C).....1126.8mW
Narrow SOIC (derate 20mW/°C above +70°C) 1600mW
QSOP (derate 9.6mW/°C above +70°C).....771.5mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 Wide SOIC	
Package Code	W16M+8
Outline Number	21-0042
Land Pattern Number	90-0107
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	71°C/W
Junction to Case (θ_{JC})	23°C/W

PACKAGE TYPE: 16 Narrow SOIC	
Package Code	S16M+11
Outline Number	21-0041
Land Pattern Number	90-0442
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	50°C/W
Junction to Case (θ_{JC})	8°C/W

PACKAGE TYPE: 16 QSOP	
Package Code	E16MS+1F
Outline Number	21-0055
Land Pattern Number	90-0167
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	103.7°C/W
Junction to Case (θ_{JC})	37°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Operating Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	V
Undervoltage Lockout Threshold	$V_{UVLO_}$	$V_{DD_}$ rising		1.45	1.58	1.71	V
Undervoltage Lockout Threshold Hysteresis	V_{UVLO_HYST}				50		mV
Supply Current (MAX14x30_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		1.2	1.9	mA
			V_{DDA} = 3.3V		1.2	1.9	
			V_{DDA} = 2.5V		1.2	1.9	
			V_{DDA} = 1.8V		1.1	1.9	
		12.5MHz square wave (Note 2)	V_{DDA} = 5V		2.1	2.7	
			V_{DDA} = 3.3V		2	2.7	
			V_{DDA} = 2.5V		2	2.7	
			V_{DDA} = 1.8V		2	2.6	
		50MHz square wave (Note 2)	V_{DDA} = 5V		5	6.6	
			V_{DDA} = 3.3V		4.6	6.1	
			V_{DDA} = 2.5V		4.5	6.0	
			V_{DDA} = 1.8V		4.5	6.0	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		8.1	11.2	
			V_{DDB} = 3.3V		7.9	11.1	
			V_{DDB} = 2.5V		7.9	11.0	
			V_{DDB} = 1.8V		7.7	10.8	
		12.5MHz square wave (Note 2)	V_{DDB} = 5V		12.8	15.9	
			V_{DDB} = 3.3V		11.1	14.2	
			V_{DDB} = 2.5V		10.2	13.4	
			V_{DDB} = 1.8V		9.4	12.4	
		50MHz square wave (Note 2)	V_{DDB} = 5V		27.2	35.4	
			V_{DDB} = 3.3V		21.7	27.8	
			V_{DDB} = 2.5V		17.6	23.0	
			V_{DDB} = 1.8V		14.4	18.9	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX14x31_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		3.4	5.3	mA
			V_{DDA} = 3.3V		3.3	5.3	
			V_{DDA} = 2.5V		3.3	5.3	
			V_{DDA} = 1.8V		3.2	5.1	
		12.5MHz square wave (Note 2)	V_{DDA} = 5V		5.6	7.1	
			V_{DDA} = 3.3V		5	6.6	
			V_{DDA} = 2.5V		4.7	6.4	
			V_{DDA} = 1.8V		4.5	6.1	
		50MHz square wave (Note 2)	V_{DDA} = 5V		12.4	16.0	
			V_{DDA} = 3.3V		10.1	13.0	
			V_{DDA} = 2.5V		9.1	11.6	
			V_{DDA} = 1.8V		8.2	10.4	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		6.5	9.2	
			V_{DDB} = 3.3V		6.4	9.1	
			V_{DDB} = 2.5V		6.3	9.1	
			V_{DDB} = 1.8V		6.2	8.9	
		12.5MHz square wave (Note 2)	V_{DDB} = 5V		10.3	12.8	
			V_{DDB} = 3.3V		8.9	11.6	
			V_{DDB} = 2.5V		8.2	11.0	
			V_{DDB} = 1.8V		7.6	10.3	
		50MHz square wave (Note 2)	V_{DDB} = 5V		22.7	29.1	
			V_{DDB} = 3.3V		17.7	23.0	
			V_{DDB} = 2.5V		14.7	19.4	
			V_{DDB} = 1.8V		11.9	15.9	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX14932_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		5.2	7.2	mA
			V_{DDA} = 3.3V		5.2	7.2	
			V_{DDA} = 2.5V		5.2	7.2	
			V_{DDA} = 1.8V		5	7.0	
		12.5MHz square wave (Note 2)	V_{DDA} = 5V		8.2	10.0	
			V_{DDA} = 3.3V		7.2	9.1	
			V_{DDA} = 2.5V		6.7	8.7	
			V_{DDA} = 1.8V		6.3	8.2	
		50MHz square wave (Note 2)	V_{DDA} = 5V		18	18.6	
			V_{DDA} = 3.3V		14.2	15.1	
			V_{DDA} = 2.5V		12.3	13.6	
			V_{DDA} = 1.8V		10.5	12.1	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		5.2	7.2	
			V_{DDB} = 3.3V		5.2	7.2	
			V_{DDB} = 2.5V		5.2	7.2	
			V_{DDB} = 1.8V		5	7.0	
		12.5MHz square wave (Note 2)	V_{DDB} = 5V		8.2	10.0	
			V_{DDB} = 3.3V		7.2	9.1	
			V_{DDB} = 2.5V		6.7	8.7	
			V_{DDB} = 1.8V		6.3	8.2	
		50MHz square wave (Note 2)	V_{DDB} = 5V		18	18.6	
			V_{DDB} = 3.3V		14.2	15.1	
			V_{DDB} = 2.5V		12.3	13.5	
			V_{DDB} = 1.8V		10.5	12.1	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V_{IH}	ENA, INA_ relative to GNDA		0.7 x V_{DDA}			V
		ENB, INB_ relative to GNDB		0.7 x V_{DDB}			
Input Low Voltage	V_{IL}	ENA, INA_ relative to GNDA	1.71V ≤ V_{DDA} ≤ 1.89V			0.6	V
			2.25V ≤ V_{DDA} ≤ 5.5V			0.8	
		ENB, INB_ relative to GNDB	1.71V ≤ V_{DDB} ≤ 1.89V			0.6	
			2.25V ≤ V_{DDB} ≤ 5.5V			0.8	
Input Hysteresis	V_{HYS}	$V_{INA_}$ relative to GNDA or $V_{INB_}$ relative to GNDB	MAX1493_A/D		410		mV
			MAX1493_B/E		410		
			MAX1493_C/F, MAX1413_C/F		80		
Input Leakage Current	I_L	$V_{INA_}$ = 0 or V_{DDA}, $V_{INB_}$ = 0 or V_{DDB}		-1		+1	µA
Input Capacitance	C_{IN}	INA_, INB_, f = 1MHz			2		pF
EN_ Pullup Current	I_{PU}			-4	-2.3	-1	µA
Output Voltage High	V_{OH}	$V_{OUTA_}$ relative to GNDA, $I_{OUTA_}$ = -4mA (Note 3)		V_{DDA} - 0.4			V
		$V_{OUTB_}$ relative to GNDB, $I_{OUTB_}$ = -4mA (Note 3)		V_{DDB} - 0.4			
Output Voltage Low	V_{OL}	$V_{OUTA_}$ relative to GNDA, $I_{OUTA_}$ = 4mA (Note 3)				0.4	V
		$V_{OUTB_}$ relative to GNDB, $I_{OUTB_}$ = 4mA (Note 3)				0.4	

Dynamic Electrical Characteristics (MAX1493_A/D)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD_}$ (Note 4)			25		kV/µs
Maximum Data Rate	DR_{MAX}			1			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTA_				1	µs
Glitch Rejection		INA_ to OUTB_, INB_ to OUTA_			32		ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		38.2	54.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		38.7	54.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		39.7	55.6	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		42.9	58.4	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		38.6	55.3	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		38.9	55.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		39.8	56.1	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		42.3	60.2	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.4	4.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.2	4.3	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	3.9	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.6	4.7	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				26.6	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				26.6	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				26.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				26.9	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				27.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				27.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				27.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				29.7	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				6.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				6.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				6.7	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				6.7	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				6.7	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				6.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				6.7	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				6.7	

Dynamic Electrical Characteristics (MAX1493_A/D) (Continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				26.6	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				26.6	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				26.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				26.9	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				27.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				27.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				27.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				29.7	
Rise Time (Figure 1)	t_R	OUTA_ / OUTB_, 10% to 90%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_ / OUTB_, 90% to 10%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			11.7	

Dynamic Electrical Characteristics (MAX1493_B/E)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD_}$ (Note 4)			25		kV/µs
Maximum Data Rate	DR_{MAX}			25			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTA_				40	ns
Glitch Rejection		INA_ to OUTB_, INB_ to OUTA_			15		ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		20.9	27.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		21.4	28.7	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		22.4	31.2	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		25.7	36.9	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		21.1	28.8	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		21.5	29.8	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		22.3	31.9	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		24.9	37.4	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.2	2.6	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.1	2.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	2.4	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.7	3.2	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				11.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				11.5	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				13.6	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				9.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				9.8	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.1	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				14.4	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				3	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				3	

Dynamic Electrical Characteristics (MAX1493_B/E) (Continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel to Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				11.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				11.5	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				13.6	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				9.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				9.8	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.1	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				14.4	
Rise Time (Figure 1)	t_R	OUTA_/ OUTB_, 10% to 90%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_/ OUTB_, 90% to 10%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, CL= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			11.7	

Dynamic Electrical Characteristics (MAX1493_C/F, MAX1413_C/F)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD_}$ (Note 4)			25		kV/µs
Maximum Data Rate	DR_{MAX}			150			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTB_				6.67	ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		5.1	7.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		5.2	8.1	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		5.8	9.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		8.1	14	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		4.9	7.4	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		5.3	8.3	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		5.9	10.2	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		8.2	14.9	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.2	1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.1	1	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	1	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.1	1	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3.0	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.1	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				2.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.4	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.9	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				0.9	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				1.2	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				1.4	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				1.6	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				0.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				1.2	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				1.4	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				1.6	

Dynamic Electrical Characteristics (MAX1493_C/F, MAX1413_C/F)) (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.1	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				2.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.4	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.9	
Rise Time (Figure 1)	t_R	OUTA_ / OUTB_, 10% to 90%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_ / OUTB_, 90% to 10%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			V_{DDA}, V_{DDB} ≤ 1.89V			11.7	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	V_{DDA}, V_{DDB} = 5.0V			140		ps
		V_{DDA}, V_{DDB} = 3.3V			130		
		V_{DDA}, V_{DDB} = 2.5V			140		
		V_{DDA}, V_{DDB} = 1.8V			160		

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		±4		kV

Note 1: All devices are 100% production tested at T_A = +125°C. Specifications over temperature are guaranteed by design.
Note 2: Not production tested. Guaranteed by design.
Note 3: All currents into the device are positive. All currents out of the device are negative.
Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

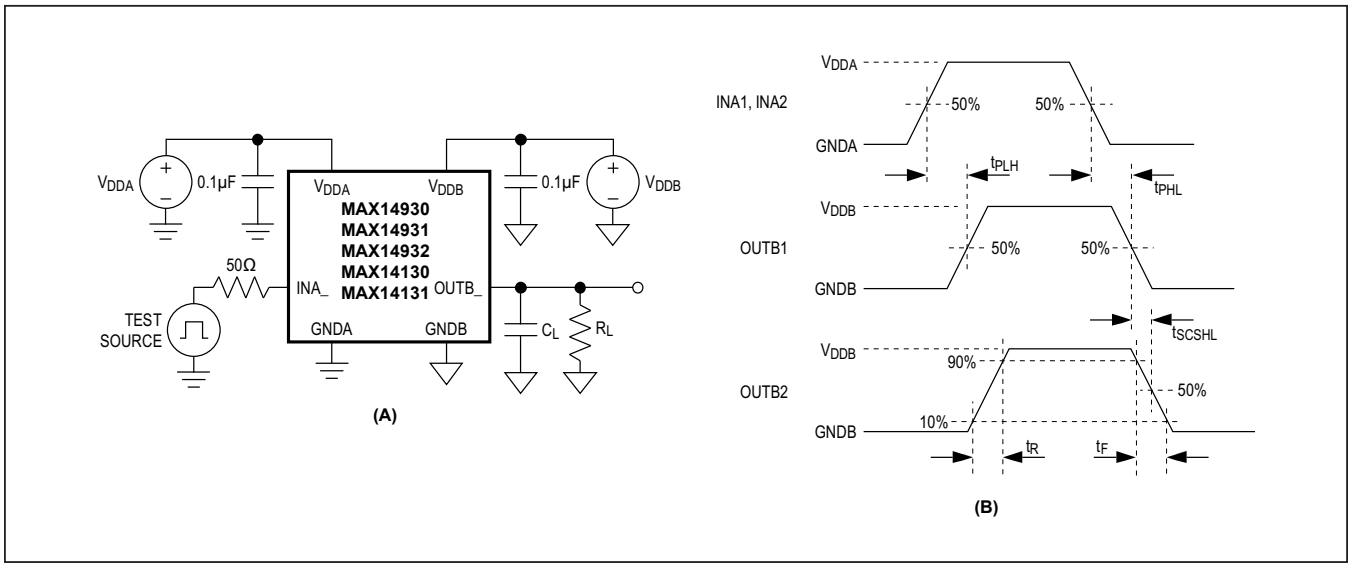


Figure 1. Test Circuit (A) and Timing Diagram (B)

Safety Regulatory Approvals

UL
The MAX14930–MAX14932 are certified under UL1577. For more details, refer to file E351759.
Rated up to 3750V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX14930–MAX14932 are certified up to 3750V$_{RMS}$ for single protection. For more details, refer to file E351759.
VDE
The MAX14930-MAX14932 are certified to DIN VDE V 0884-11: 2017-01. For details, see file ref. 5015017-4880-0001/272147/TL7/SCT. Basic Insulation, Maximum Transient Isolation Voltage 4600V$_{PK}$, Maximum Repetitive Peak Isolation Voltage 630V$_{PK}$

These couplers are suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

IEC Insulation Testing

TUV
The MAX14930–MAX14932 are tested under TUV.
IEC 60950-1: Up to 630V$_{PK}$ (443V$_{RMS}$) working voltage for basic insulation.
IEC 61010-1 (ed. 3): Up to 443V$_{RMS}$ working voltage for basic insulation. For details, see Technical Report number 095-72100581-100.
IEC 60601-1 (ed. 3): For details, see Technical Report number 095-72100581-200.
Basic Insulation 1 MOOP, 630V$_{PK}$ (443V$_{RMS}$)
Withstand Isolation Voltage (V$_{ISO}$) for 60s, 2750V$_{RMS}$

MAX14930–MAX14932 Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)	443	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 5)	4600	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 5, 6)	2750	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (Note 5, 8)	10	kV
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 9)	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
		Narrow SOIC	4	
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
		Narrow SOIC	4	
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

MAX14130–MAX14131 Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	795	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)	424	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)	300	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 5)	1700	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 5, 7)	1000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (Note 5, 8)	4	kV
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 9)	2	pF
Minimum Creepage Distance	CPG	QSOP	4	mm
Minimum Clearance Distance	CLR	QSOP	4	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	563	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 5: V_{ISO}, V_{IOTM}, V_{IOSM}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 6: MAX14930–MAX14932 are qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 7: MAX14130–MAX14131 V_{ISO} is production tested at 720V_{RMS} for 1 second and guaranteed by design for 1kV$_{RMS}$.
Note 8: Devices are immersed in oil during surge characterization.
Note 9: Capacitance is measured with all pins on field-side and logic-side tied together.

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX14930–MAX14932 and MAX14130–MAX14131 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. Table 1 shows the safety limits for the MAX14930–MAX14932 and MAX14130–MAX14131.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section of the datasheet. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 2 to Figure 4 show the thermal derating curves for the safety power limiting of the devices and Figure 5 shows the thermal derating curve for the safety current limiting of the devices. Ensure that the junction temperature does not exceed 150°C.

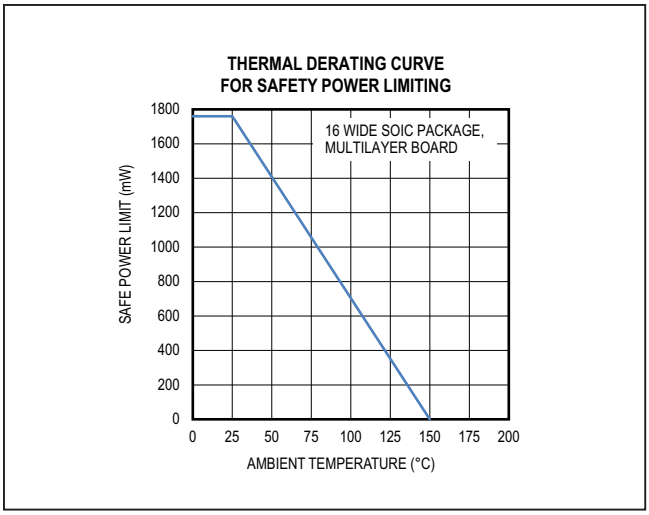


Figure 2. Thermal Derating Curve for Safety Power Limiting - Wide SOIC

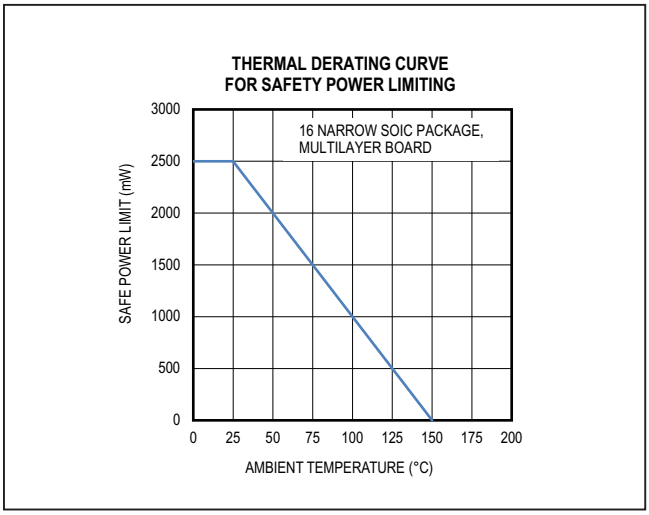


Figure 3. Thermal Derating Curve for Safety Power Limiting - Narrow SOIC

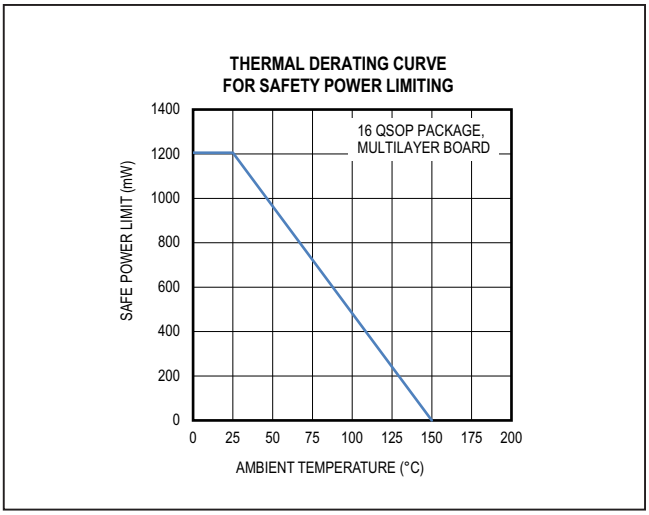


Figure 4. Thermal Derating Curve for Safety Power Limiting - QSOP

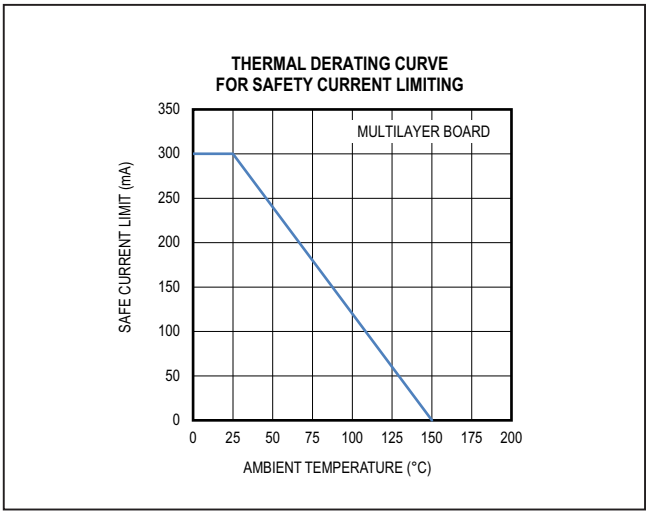


Figure 5. Thermal Derating Curve for Safety Current Limiting

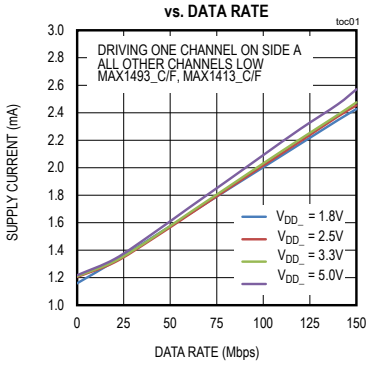
Table 1. Safety Limiting Values for the MAX14930–MAX14932 and MAX14130–MAX14131

PARAMETER	SYMBOL	TEST CONDITIONS		MAX	UNITS
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C		300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	Wide SOIC	1760	mW
			Narrow SOIC	2500	
			QSOP	1205	
Maximum Safety Temperature	T_S			150	°C

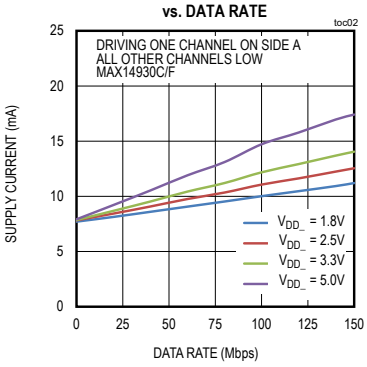
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

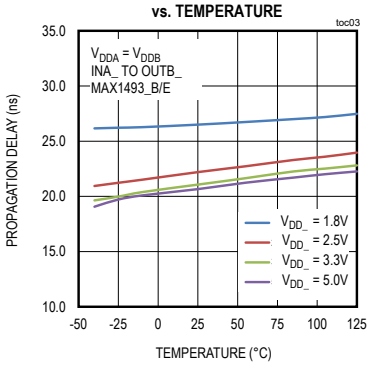
SIDE A SUPPLY CURRENT vs. DATA RATE



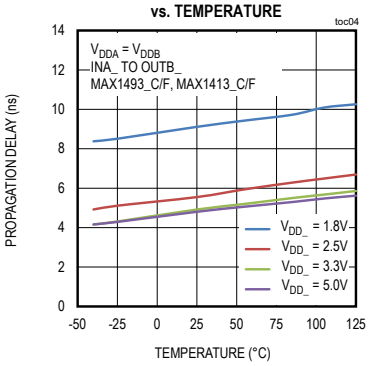
SIDE B SUPPLY CURRENT vs. DATA RATE



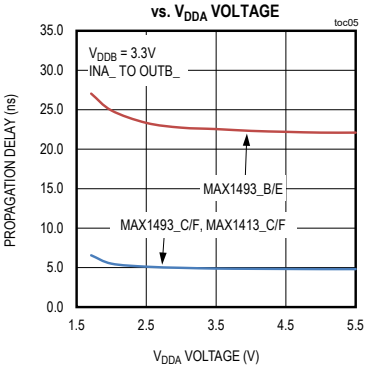
PROPAGATION DELAY vs. TEMPERATURE



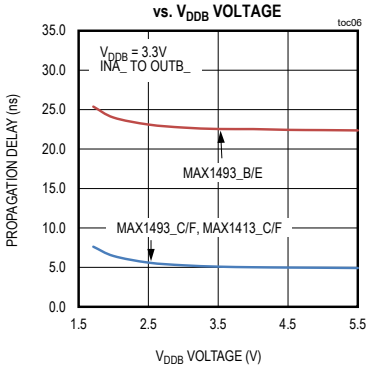
PROPAGATION DELAY vs. TEMPERATURE



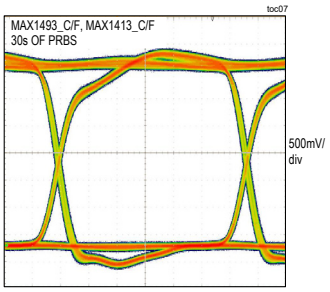
PROPAGATION DELAY vs. V_{DDA} VOLTAGE



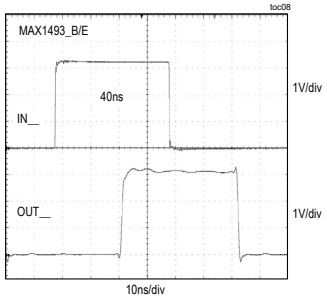
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



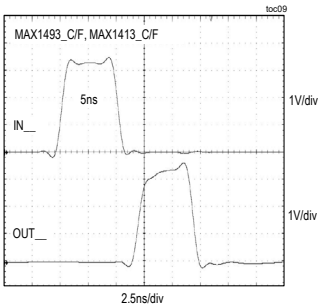
EYE DIAGRAM at 150Mbps



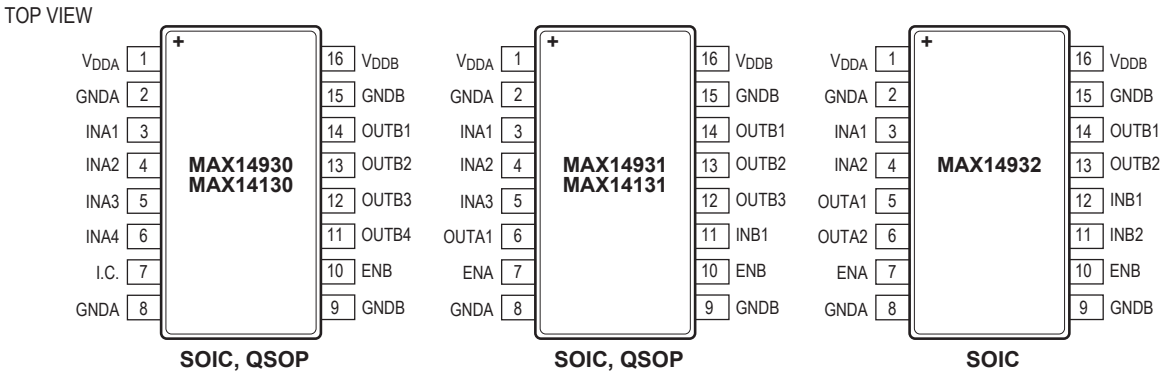
MINIMUM PULSE WIDTH



MINIMUM PULSE WIDTH



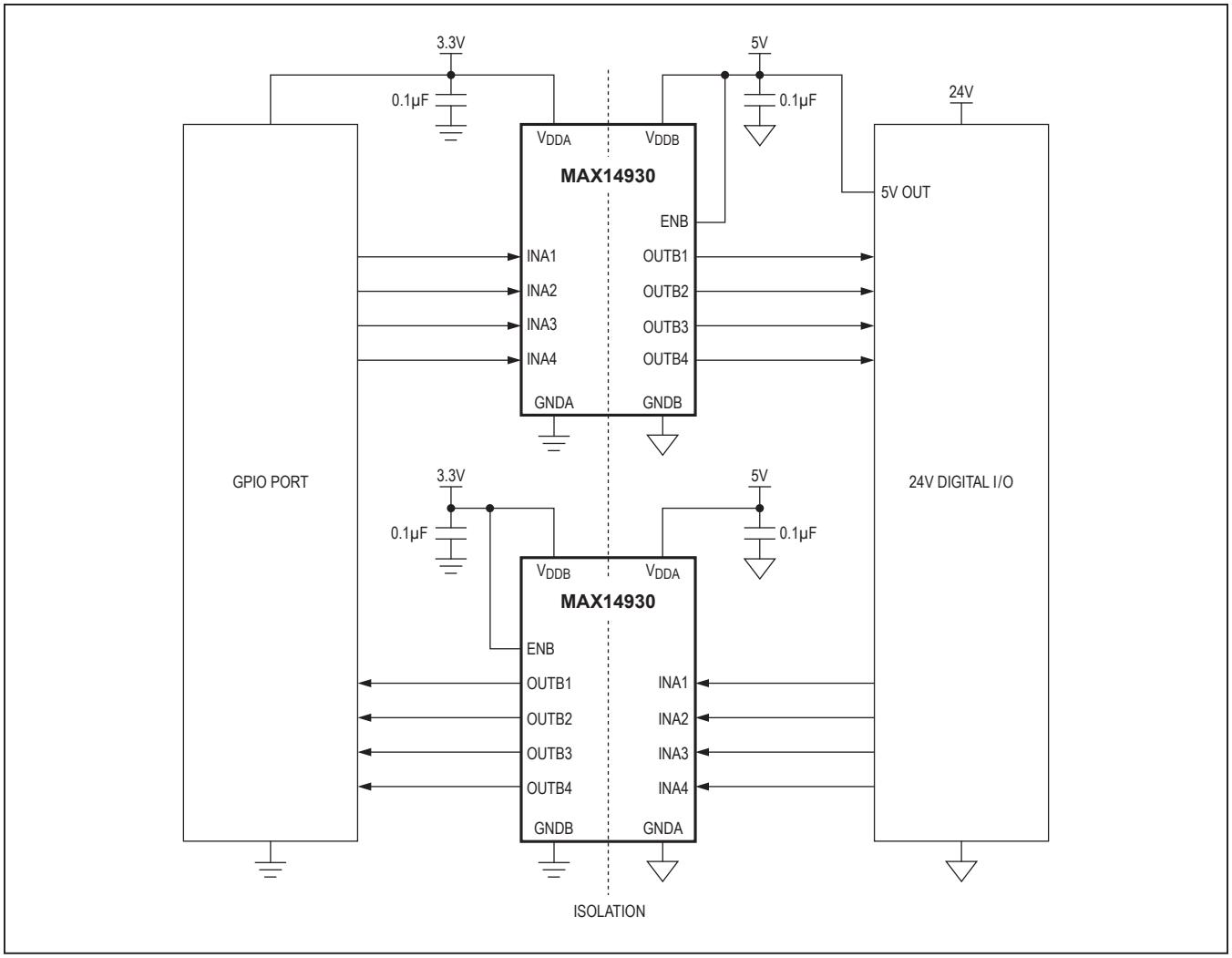
Pin Configurations



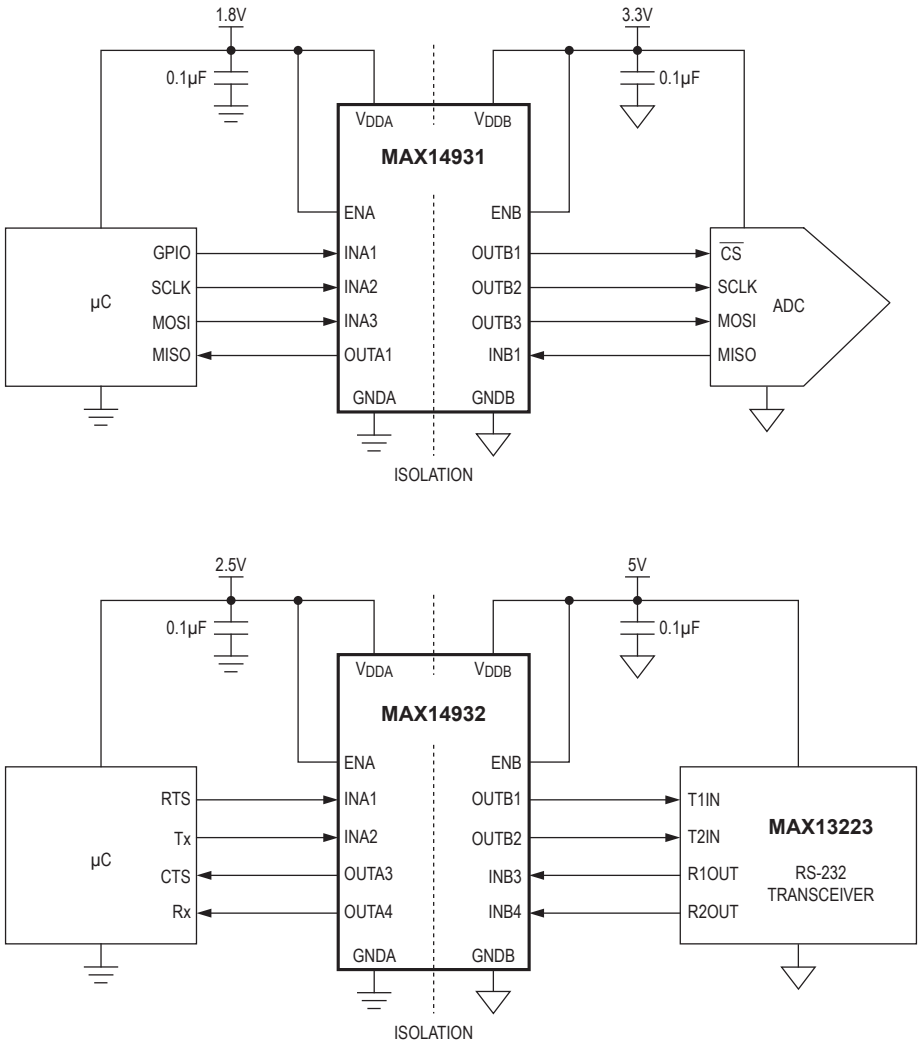
Pin Description

PIN			NAME	FUNCTION	VOLTAGE RELATIVE TO
MAX14x30	MAX14x31	MAX14932			
1	1	1	VDDA	Power Supply. Bypass VDDA with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDA
2, 8	2, 8	2, 8	GNDA	Ground Reference for Side A	—
3	3	3	INA1	Logic Input 1 on Side A. INA1 corresponds to OUTB1.	GNDA
4	4	4	INA2	Logic Input 2 on Side A. INA2 corresponds to OUTB2.	GNDA
5	5	—	INA3	Logic Input 3 on Side A. INA3 corresponds to OUTB3.	GNDA
6	—	—	INA4	Logic Input 4 on Side A. INA4 corresponds to OUTB4.	GNDA
7	—	—	I.C.	Internally Connected. Leave unconnected or connect to GNDA or VDDA.	—
—	6	5	OUTA1	Logic Output 1 on Side A	GNDA
—	—	6	OUTA2	Logic Output 2 on Side A	GNDA
—	7	7	ENA	Active-High Enable for Side A. ENA has an internal 2µA pullup to VDDA.	GNDA
9, 15	9, 15	9, 15	GNDB	Ground Reference for Side B	—
10	10	10	ENB	Active-High Enable for Side B. ENB has an internal 2µA pullup to VDDB.	GNDB
11	—	—	OUTB4	Logic Output 4 on Side B	GNDB
—	11	12	INB1	Logic Input 1 on Side B. INB1 corresponds to OUTA1.	GNDB
—	—	11	INB2	Logic Input 2 on Side B. INB2 corresponds to OUTA2.	GNDB
12	12	—	OUTB3	Logic Output 3 on Side B	GNDB
13	13	13	OUTB2	Logic Output 2 on Side B	GNDB
14	14	14	OUTB1	Logic Output 1 on Side B	GNDB
16	16	16	VDDB	Power Supply. Bypass VDDB with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDB

Typical Application Circuits



Typical Application Circuits (continued)



Detailed Description

The MAX14930–MAX14932 and MAX14130–MAX14131 are a family of 4-channel digital isolators. The MAX14930–MAX14932 family transfers digital signals between circuits with different power domains. The devices are rated for up to 2.75kV$_{RMS}$ isolation voltage for 60 seconds. The MAX14130–MAX14131 are rated for up to 1kV$_{RMS}$ isolation voltage for 60 seconds. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

The devices offer three unidirectional channel configurations for design convenience. The MAX14x30 features four channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX14x31 has three channels transmitting data in one direction and one channel transmitting in the opposite direction, making it ideal for applications such as isolated SPI and RS-485 communication. The MAX14932 provides further design flexibility with two channels in each direction for isolated RS-232 or other applications.

Devices are available with data rates from DC up to 1Mbps (A/D versions), 25Mbps (B/E versions), or 150Mbps (C/F versions). Each device can also be ordered with default-high or default-low outputs. This is the state an output will go to when the input side of the device is unpowered.

The devices have two supply inputs, V_{DDA} and V_{DDB}, that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX14930–MAX14932 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX14930–MAX14932 family provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 630V$_{PEAK}$ of continuous isolation is supported, as well as transient differences of up to 2.75kV$_{RMS}$ for up to 60 seconds. The MAX14130–MAX14131 family provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 424V$_{PEAK}$ of continuous isolation is supported, as well as transient differences of up to 1kV$_{RMS}$ for up to 60 seconds.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX14930–MAX14932 and MAX14130–MAX14131 family to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX14930–MAX14932 and MAX14130–MAX14131 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 1Mbps (A/D versions), 25Mbps (B/E versions), or 150Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the status of the inputs (Table 2). Figure 6 through Figure 9 show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Conditions

V_{IN}	V_{DDA}	V_{DDB}	ENA	ENB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	1	1	1	1
			0	0	Hi-Z	Hi-Z
0	Powered	Powered	1	1	0	0
			0	0	Hi-Z	Hi-Z
X	Undervoltage	Powered	1	1	Default	Default
			0	0	Hi-Z	Hi-Z
X	Powered	Undervoltage	1	1	Default	Default
			0	0	Hi-Z	Hi-Z

Note: *EN_ = 0 (Hi-Z Mode) takes precedence over the default value.*

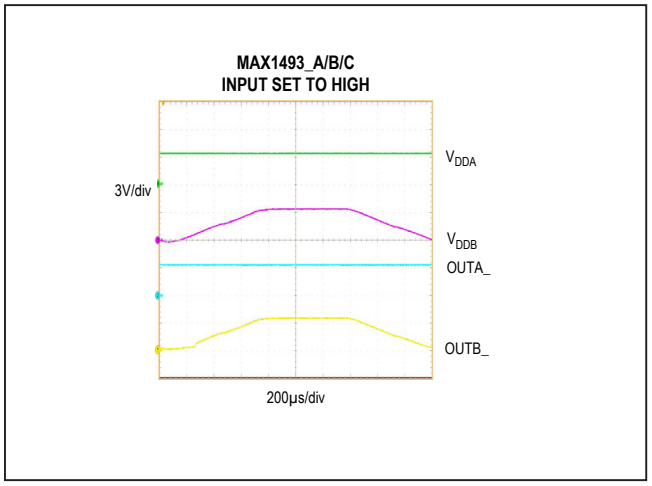


Figure 6. Undervoltage Lockout Behavior (MAX1493_ A/B/C High)

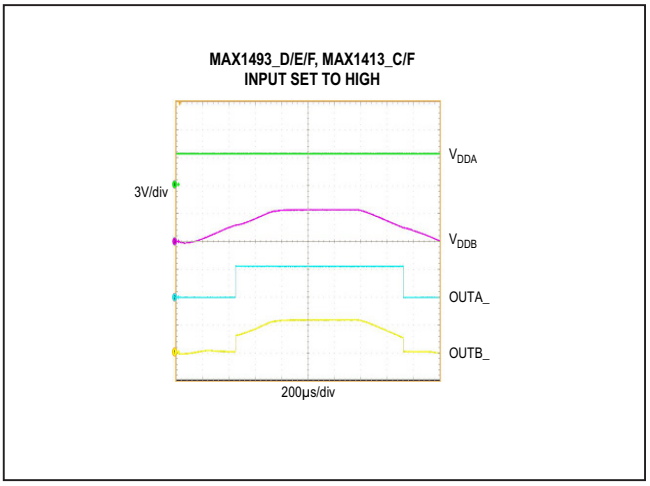


Figure 8. Undervoltage Lockout Behavior (MAX1493_ D/E/F, MAX1413_C/F High)

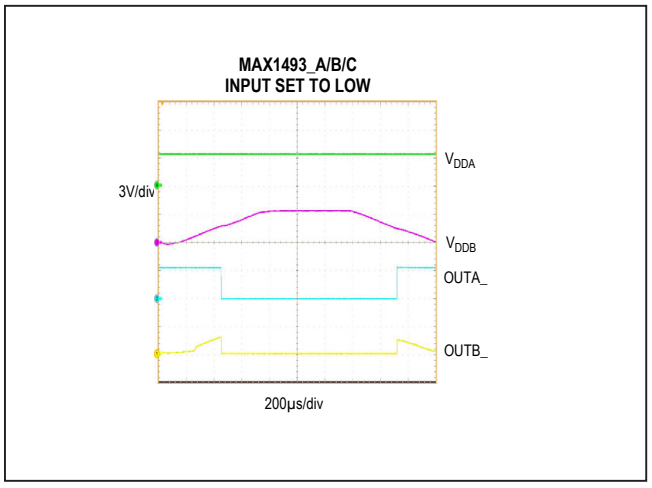


Figure 7. Undervoltage Lockout Behavior (MAX1493_ A/B/C Low)

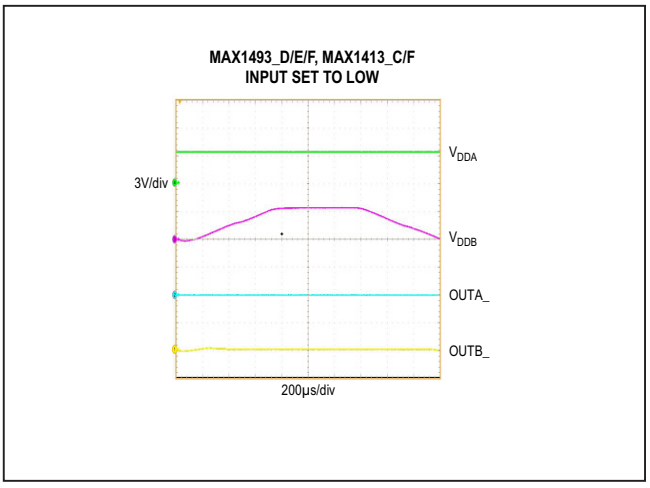


Figure 9. Undervoltage Lockout Behavior (MAX1493_ D/E/F, MAX1413_C/F Low)

Applications Information

Power-Supply Sequencing

The MAX14930–MAX14932 and MAX14130–MAX14131 do not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

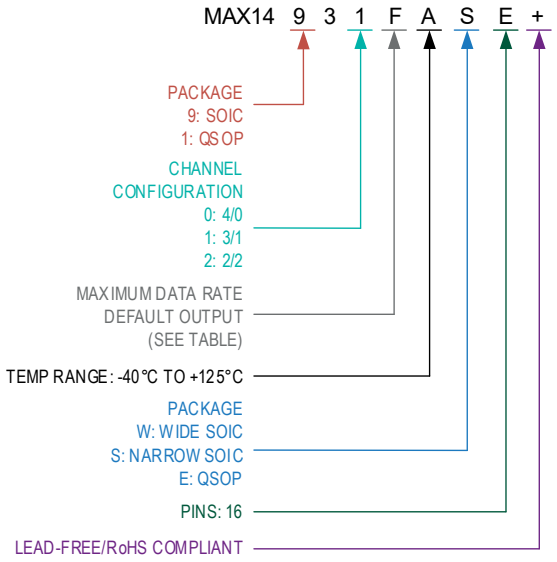
To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX14930–MAX14932 and MAX14130–MAX14131 free from ground and signal planes. Any galvanic or metallic connection between the Side A and Side B defeats the isolation.

Product Selector Guide



DEVICE CONFIGURATION	MAX DATA RATE		
	1Mbps	25Mbps	150Mbps
DEFAULT-HIGH OUTPUT	A	B	C
DEFAULT-LOW OUTPUT	D	E	F

Ordering Information

PART	CHANNEL CONFIGURATION	DATA RATE (Mbps)	OUTPUT	ISOLATION VOLTAGE (kV$_{RMS}$)	TEMP RANGE	PIN-PACKAGE
MAX14930AASE+	4/0	1	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930AAWE+	4/0	1	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14930BASE+	4/0	25	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930BAWE+	4/0	25	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14930CASE+	4/0	150	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930CAWE+	4/0	150	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14930DASE+	4/0	1	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930DAWE+	4/0	1	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14930EASE+	4/0	25	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930EAWE+	4/0	25	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14930FASE+	4/0	150	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14930FAWE+	4/0	150	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931AASE+	3/1	1	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931AAWE+	3/1	1	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931BASE+	3/1	25	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931BAWE+	3/1	25	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931CASE+	3/1	150	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931CAWE+	3/1	150	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931DASE+	3/1	1	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931DAWE+	3/1	1	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931EASE+	3/1	25	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931EAWE+	3/1	25	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14931FASE+	3/1	150	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14931FAWE+	3/1	150	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932AASE+	2/2	1	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932AAWE+	2/2	1	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932BASE+	2/2	25	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932BAWE+	2/2	25	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932CASE+	2/2	150	Default High	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932CAWE+	2/2	150	Default High	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932DASE+	2/2	1	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932DAWE+	2/2	1	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932EASE+	2/2	25	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932EAWE+	2/2	25	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14932FASE+	2/2	150	Default Low	2.75	-40°C to +125°C	16 Narrow SOIC
MAX14932FAWE+	2/2	150	Default Low	2.75	-40°C to +125°C	16 Wide SOIC
MAX14130FAEE+	4/0	150	Default Low	1	-40°C to +125°C	16 QSOP
MAX14130FAEE+T	4/0	150	Default Low	1	-40°C to +125°C	16 QSOP
MAX14131CAEE+	3/1	150	Default High	1	-40°C to +125°C	16 QSOP
MAX14131FAEE+	3/1	150	Default Low	1	-40°C to +125°C	16 QSOP
MAX14131FAEE+T	3/1	150	Default Low	1	-40°C to +125°C	16 QSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	12/14	Changed future product status on several parts in the Ordering Information/Selector Guide table. Changed “basic insulation” to “single protection” in *Safety Regulatory Approvals* table.	13, 22
2	3/15	Changed future product status for MAX14930FAWE+, MAX14931DASE+, MAX-14932AAWE+, MAX14932BASE+, MAX14932DAWE+, MAX14932EAWE+, and MAX14932FAWE+	22
3	5/15	Added UL/cUL, TUV information, and fixed corresponding isolation parameters	1, 13-14, 16
4	10/15	Added 3.75kV versions: MAX14930FASE+CZ0 and MAX14931FASE+CZ1	1, 13, 14, 17-19, 22, 23
5	4/16	Fixed typos, updated *Safety Regulatory Approvals* table, and updated *Ordering Information and Selection Guide*	1, 13, 14, 22
6	5/16	Moved TUV information to new *IEC Insulation* section and updated Ordering Information table	1, 13, 22
7	7/16	Added MAX14130 and MAX14131 versions in QSOP package	1–4, 6, 11, 12, 14–16, 19–24
8	1/17	Updated Figure 1 text, removed VDE pending status, and removed future product status from MAX14131FAEE+T and MAX14131FAEE+T	13, 15, 23
8.1		Corrected typos	23
9	11/20	Updated *General Description, Dynamic Electrical Characteristics (MAX1493_A/D), Dynamic Electrical Characteristics (MAX1493_B/E), Dynamic Electrical Characteristics (MAX1493_C/F), Safety Regulatory Approvals, Typical Operating Circuits,* and *Layout Considerations* sections; added *Safety Limits* and *Product Selector Guide* sections; added new Figure 2–5 and renumbered subsequent figures; added Table 1 and renumbered subsequent tables; added *Product Selector Guide*	1, 5–10, 14– 24
10	8/21	Updated *Benefits and Features* section and Insulation Characteristics Table	1, 15
11	3/22	Updated *Benefits and Features* section, DC Electrical Characteristics table, Dynamic Electrical Characteristics table, MAX14130-14131 Insulation Characteristics table, Typcial Operating Characteristics, Figure 8, and Figure 9; Added MAX14131CAEE+ to *Ordering Information* table	1, 6, 11, 12, 13, 15, 17, 22, 24

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