

AM79C984A

Enhanced Integrated Multiport Repeater (eIMR)

The enhanced Integrated Multiport Repeater (eIMR) device is a VLSI integrated circuit that provides a system-level solution to designing non-managed multiport repeaters. The device integrates the repeater functions specified in Section 9 of the IEEE 802.3 standard and Twisted Pair Transceiver functions complying with the 10BASE-T standard.

The device is fabricated in CMOS technology and requires a single +5-V supply.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am79C984A

enhanced Integrated Multiport Repeater (eIMR™)

DISTINCTIVE CHARACTERISTICS

- Repeater functions comply with IEEE 802.3 Repeater Unit specifications
- Four integral 10BASE-T transceivers with on-chip filtering that eliminate the need for external filter modules on the 10BASE-T transmit-data (TXD) and receive-data (RXD) lines
- One Reversible Attachment Unit Interface (RAUI™) port that can be used either as a standard IEEE-compliant AUI port for connection to a Medium Attachment Unit (MAU), or as a reversed port for direct connection to a Media Access Controller (MAC)
- Low cost suitable for non-managed multiport repeater designs
- Expandable to increase number of repeater ports with support for up to seven eIMR devices without the need for an external arbiter
- All ports can be individually isolated (partitioned) in response to excessive collision conditions or fault conditions.
- Full LED support for individual port status LEDs and network utilization LEDs
- Programmable extended distance mode on the RXD lines, allowing connection to cables longer than 100 meters
- Twisted Pair Link Test capability conforming to the 10BASE-T standard. The Link Test function and the transmission of Link Test pulses can be optionally disabled through the control port to allow devices that do not implement the Link Test function to work with the eIMR device.
- Programmable option of automatic polarity detection and correction permits automatic recovery due to wiring errors
- Full amplitude and timing regeneration for retransmitted waveforms
- CMOS device with a single +5-V supply

GENERAL DESCRIPTION

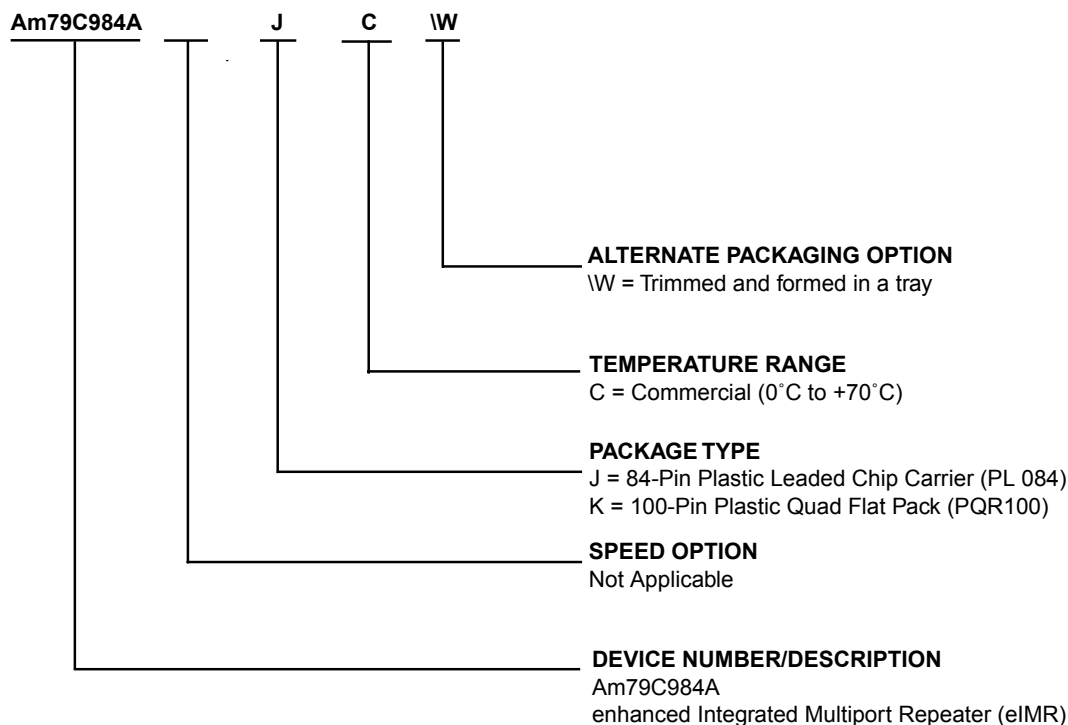
The enhanced Integrated Multiport Repeater (eIMR) device is a VLSI integrated circuit that provides a system-level solution to designing non-managed multiport repeaters. The device integrates the repeater functions specified in Section 9 of the IEEE 802.3 standard and Twisted Pair Transceiver functions complying with the 10BASE-T standard.

The eIMR device provides four Twisted Pair (TP) ports and one RAUI port for direct connection to a MAC. The total number of ports per repeater unit can be increased by connecting multiple eIMR devices through their expansion ports, hence, minimizing the total cost per repeater port.

The device is fabricated in CMOS technology and requires a single +5-V supply.

ORDERING INFORMATION**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

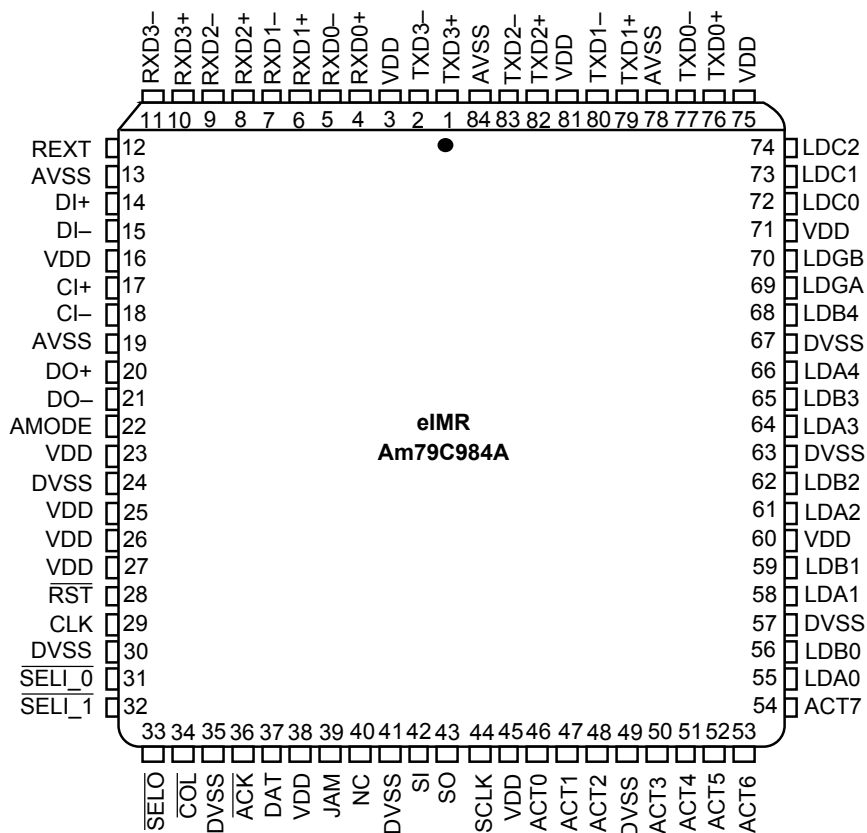


Valid Combinations	
Am79C984A	JC, KC\W

Valid Combinations

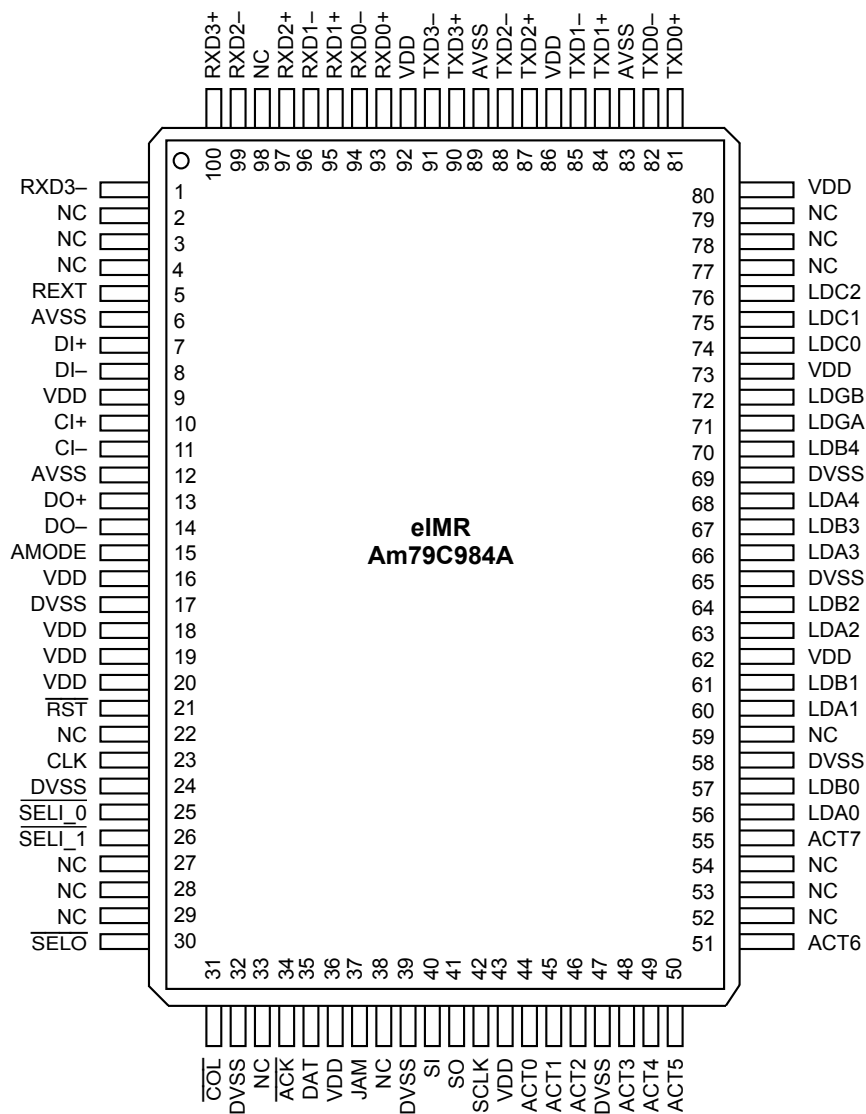
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

CONNECTION DIAGRAM (PL 084)



20650B-2

CONNECTION DIAGRAM (PQR100)



20650B-3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature Under Bias 0°C to $+70^{\circ}\text{C}$
 Supply Voltage referenced to

AV_{SS} or DV_{SS} (AV_{DD} , DV_{DD}) -0.3 V to $+6.0\text{ V}$

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect reliability. Programming conditions may differ.

OPERATING RANGES**Commercial (C) Devices**

Temperature (T_A) 0°C to $+70^{\circ}\text{C}$

Supply Voltages (V_{DD}) $+5\text{ V} \pm 5\%$

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	$\text{V}_{\text{SS}} = 0.0\text{ V}$	-0.5	0.8	V
V_{IH}	Input HIGH Voltage	$\text{V}_{\text{SS}} = 0.0\text{ V}$	2.0	$0.5 + \text{V}_{\text{DD}}$	V
V_{OL}	Output LOW Voltage	$I_{\text{OL}} = 4.0\text{ mA}$	$-$	0.4	V
V_{OH}	Output HIGH Voltage	$I_{\text{OH}} = -0.4\text{ mA}$	2.4	$-$	V
I_{IL}	Input Leakage Current	$\text{V}_{\text{SS}} < \text{V}_{\text{IN}} < \text{V}_{\text{DD}}$	$-$	10	μA
I_{ILSTR}	Input Leakage Current for STR pin	$\text{V}_{\text{SS}} < \text{V}_{\text{IN}} < \text{V}_{\text{DD}}$	$-$	50	μA
V_{OLOD}	Open Drain Output LOW Voltage (LED pins)	$I_{\text{OLOD}} = 12\text{ mA}$	$-$	0.4	V
AUI Ports					
I_{IAXD}	Input Current at $\text{DI}_{\pm}$ and $\text{CI}_{\pm}$ Pairs	$\text{V}_{\text{SS}} < \text{V}_{\text{IN}} < \text{V}_{\text{DD}}$	-500	500	μA
V_{AICM}	$\text{DI}_{\pm}$, $\text{CI}_{\pm}$ Open Circuit Input Voltage Range	$I_{\text{IN}} = 0$	$\text{V}_{\text{DD}} - 3.0$	$\text{V}_{\text{DD}} - 1.0$	V
V_{AIDV}	Differential Mode Input Voltage Range (DI , CI)	$\text{V}_{\text{DD}} = 5.0\text{ V}$	-2.5	$+2.5$	V
V_{ASQ}	DI , CI Squelch Threshold	$-$	-275	-160	mV
V_{ATH}	DI Switching Threshold	(Note 1)	-35	$+35$	mV
V_{AOD}	Differential Output Voltage $ (\text{DO}+) - (\text{DO}) $	$R_L = 78\ \Omega$	620	1100	mV
V_{AOC}	Differential Output Voltage $ (\text{CI}+) - (\text{CI}-) $ (Reverse Mode)	$R_L = 78\ \Omega$	620	1100	mV
V_{AODI}	DO Differential Output Voltage Imbalance	$R_L = 78\ \Omega$	-25	$+25$	mV
V_{AODOFF}	DO Differential Idle Output Voltage	$R_L = 78\ \Omega$	-40	$+40$	mV
I_{AODOFF}	DO Differential Idle Output Current	$R_L = 78\ \Omega$ (Note 1)	-1.0	$+1.0$	mA
V_{AOCM}	$\text{DO}+$, $\text{DO}-$ Common Mode Output Voltage	$R_L = 78\ \Omega$	2.5	V_{DD}	V
Twisted Pair Ports					
I_{IRXD}	Input Current at $\text{RXD}_{\pm}$ and $\text{CI}_{\pm}$ Pairs	$\text{AV}_{\text{SS}} < \text{V}_{\text{IN}} < \text{V}_{\text{DD}}$	-500	500	μA
R_{RXD}	RXD Differential Input	(Note 1)	10	$-$	$\text{k}\Omega$
V_{TIVB}	$\text{RXD}+$, $\text{RXD}-$ Open Circuit Input Voltage (bias)		$\text{V}_{\text{DD}} - 3.0$	$\text{V}_{\text{DD}} - 1.5$	V
V_{TID}	Differential Mode Input Range (RXD)	$\text{V}_{\text{DD}} = 5.0\text{ V}$	-3.1	$+3.1$	V

DC CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Ports (Continued)					
V _{TSQ+}	RXD Positive Squelch Threshold (peak)	Sinusoid 5 MHz < f < 10 MHz	300	520	mV
V _{TSQ-}	RXD Negative Squelch Threshold (peak)	Sinusoid 5 MHz < f < 10 MHz	-520	-300	mV
V _{THS+}	RXD Post-Squelch Positive Threshold (peak)	Sinusoid 5 MHz < f < 10 MHz	150	293	mV
V _{THS-}	RXD Post-Squelch Negative Threshold (peak)	Sinusoid 5 MHz < f < 10 MHz	-293	-150	mV
V _{LTSQ+}	RXD Positive Squelch Threshold (peak) - Extended Distance Mode	Sinusoid 5 MHz < f < 10 MHz	180	365	mV
V _{LTSQ-}	RXD Negative Squelch Threshold (peak) - Extended Distance Mode	Sinusoid 5 MHz < f < 10 MHz	-365	-180	mV
V _{LTHS+}	RXD Post-Squelch Positive Threshold - Extended Distance Mode	Sinusoid 5 MHz < f < 10 MHz	90	175	mV
V _{LTHS-}	RXD Post-Squelch Negative Threshold - Extended Distance Mode	Sinusoid 5 MHz < f < 10 MHz	-175	-90	mV
V _{RXDTH}	RXD Switching Threshold	(Note 1)	-60	60	mV
Power Supply Current					
I _{DD}	Power Supply Current (Idle) (Note 2)	CLK = 20 MHz V _{DD} = +5.25V	-	100	mA
	Power Supply Current (Transmitting)	CLK = 20 MHz V _{DD} = +5.25V	-	350	mA

Notes:

1. Parameter not tested.
2. LED current not included. Maximum current rating on LED drivers is 12 mA.

SWITCHING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock and Reset Timing					
t_{CLK}	CLK Clock Period		49.995	50.005	ns
t_{CLKH}	CLK Clock High		20	30	ns
t_{CLKL}	CLK Clock Low		20	30	ns
t_{CLKR}	CLK Rise Time		–	10	ns
t_{CLKF}	CLK Fall Time		–	10	ns
t_{PRST}	Reset Pulse Width after Power On		150	–	μs
t_{RST}	Reset Pulse Width		4	–	μs
t_{RSTSET}	Reset HIGH Setup Time with respect to CLK		15	–	ns
t_{RSTHLD}	Reset LOW Hold Time		0	–	ns
t_{XRS}	AMODE, $\overline{SEL}_0$, and SI_D Setup Time to Rising Edge of RST		0	–	ns
t_{XRH}	AMODE, $\overline{SEL}_0$, and SI_D Hold Time from Rising Edge of RST		400	–	ns
AUI Port Timing					
t_{DOTD}	CLK Rising Edge to DO Toggle		–	30	ns
t_{DOTR}	DO+, DO– Rise Time (10% to 90%)		–	7.0	ns
t_{DOTF}	DO+, DO– Fall Time (90% to 10%)		–	7.0	ns
t_{DORM}	DO+, DO– Rise and Fall Time Mismatch		–	1.0	ns
t_{DOETD}	DO± End of Transmission		275	375	ns
t_{PWODI}	DI Pulse Width Accept/Reject Threshold	$ V_{IN} > V_{ASQ} $ (Note 2)	15	45	ns
t_{PWKDI}	DI Pulse Width Not to Turn-off Internal Carrier Sense	$ V_{IN} > V_{ASQ} $ (Note 3)	136	200	ns
t_{PWOCI}	CI Pulse Width Accept/Reject Threshold	$ V_{IN} > V_{ASQ} $ (Note 4)	10	26	ns
t_{PWKCI}	CI Pulse Width Not to Turn-off Threshold	$ V_{IN} > V_{ASQ} $ (Note 5)	75	160	ns
t_{CITR}	CI Rise Time (In Reverse Mode)		–	7.0	ns
t_{CITF}	CI Fall Time (In Reverse Mode)		–	7.0	ns
t_{CIRM}	CI+, CI– Rise and Fall Time Mismatch (AUI in Reverse Mode)		–	1.0	ns
Expansion Bus Timing					
t_{CLKHRL}	CLK HIGH to $\overline{SELO}$ Driven LOW	$C_L = 50$ pF	15	30	ns
t_{CLKHRH}	CLK HIGH to $\overline{SELO}$ Driven HIGH	$C_L = 50$ pF	15	30	ns
t_{CLKHDR}	CLK HIGH to DAT/JAM Driven	$C_L = 100$ pF	14	30	ns
t_{CLKHDZ}	CLK HIGH to DAT/JAM Not Driven	$C_L = 100$ pF	14	30	ns
t_{DJSET}	DAT/JAM Setup Time to CLK		10	–	ns
t_{DJHOLD}	DAT/JAM Hold Time from CLK		9	–	ns
t_{CASET}	$\overline{COL}/\overline{ACK}$ Setup Time to CLK		10	–	ns
t_{CAHLD}	$\overline{COL}/\overline{ACK}$ Hold Time from CLK		9	–	ns
$t_{SCLKHLD}$	SI, SCLK Hold Time		50	–	ns

SWITCHING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Port Timing					
t_{TXTD}	CLK Rising Edge to TXD $\pm$ Transition Delay		–	50	ns
t_{TETD}	Transmit End of Transmission		250	375	ns
t_{PWKRD}	RXD Pulse Width Maintain/Turn-off Threshold	$ V_{\text{IN}} > V_{\text{THS}} $ (Note 6)	136	200	ns
t_{PERLP}	Idle Signal Period		8	24	ms
t_{PWLP}	Idle Link Test Pulse Width		75	120	ns
Control Port Timing					
t_{SCLK}	SCLK Clock Period		100	–	ns
t_{SCLKH}	SCLK Clock HIGH		30	–	ns
t_{SCLKL}	SCLK Clock LOW		30	–	ns
t_{SCLKR}	SCLK Clock Rise Time		–	10	ns
t_{SCLKF}	SCLK Clock Fall Time		–	10	ns
t_{SISSET}	SI Input Setup Time to SCLK Rising Edge		10	–	ns
t_{SIHLD}	SI Input Hold Time from SCLK Rising Edge		10	–	ns
t_{SODLY}	SO Output Delay from SCLK Rising Edge	$C_L = 100 \text{ pF}$	–	40	ns

Notes:

1. Parameter not tested.
2. DI pulses narrower than $t_{\text{PWODI}}(\text{min})$ will be rejected; pulses wider than $t_{\text{PWODI}}(\text{max})$ will turn internal DI carrier sense on.
3. DI pulses narrower than $t_{\text{PWKDI}}(\text{min})$ will maintain internal DI carrier on; pulses wider than $t_{\text{PWKDI}}(\text{max})$ will turn internal DI carrier sense off.
4. CI pulses narrower than $t_{\text{PWOCI}}(\text{min})$ will be rejected; pulses wider than $t_{\text{PWOCI}}(\text{max})$ will turn internal CI carrier sense on.
5. CI pulses narrower than $t_{\text{PWKCI}}(\text{min})$ will maintain internal CI carrier on; pulses wider than $t_{\text{PWKCI}}(\text{max})$ will turn internal CI carrier sense off.
6. RXD pulses narrower than $t_{\text{PWKRD}}(\text{min})$ will maintain internal RXD carrier sense on; a pulse wider than $t_{\text{PWKRD}}(\text{max})$ will turn RXD carrier sense off.